Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A system development method comprising:

a step of inputting program descriptions which define a plurality of devices by employing a Java program language capable of describing parallel operations;

a step of converting the input program descriptions into an intermediate expression;

a step of generating parameters which satisfy a real-time restriction, for the intermediate expression; and

a step of synthesizing circuit descriptions which are based on a hardware description language, on the basis of the generated parameters;

wherein the program descriptions define the devices on a single bus by using a run method of the Java program language, and define clock synchronizations of the device by using barrier synchronizations,

wherein in the run method, program codes which are to be executed in a thread constituting a multi-thread are described,

imposing an inhibition of dynamic instantiation restriction and an inhibition of a start method call from the run method restriction on the program descriptions by employing a Java program language,

wherein the intermediate expression comprises a temporal automaton and a concurrent control flow flag generated by expressing the start of the "synchronized" operation as a node which is labeled as "Begin sync" and the end thereof as a node which is labeled as

"End sync",

wherein the temporal automaton is converted from the concurrent control flow flag in which a part held between description the "Begin sync" and the "End sync" are identified, and is set as a "sync" block, a clock boundary node which does not exist in the "sync" block is set as a state allotment candidate, the state allotment candidates obtained are allotted so as not to concur, and a section from each state to another state is traversed by a Depth First Search, a transition corresponding to the "sync" block is detected for the automaton and is set as a "sync" transition, and the number of states is decreased by collecting into one transition, transitions which are not successive transitions, and

wherein parametric model checking is performed using the temporal automaton for the parameter generation.

2. – 5. (Canceled)

6. (Currently Amended) A data processing system comprising:

a computer;

said computer inputting program descriptions which define a plurality of devices by employing a Java program language capable of describing parallel operations, converting the input program descriptions into an intermediate expression, generating parameters which satisfy a real-time restriction, for the intermediate expression, and synthesizing circuit descriptions which are based on a hardware description language, on the basis of the generated parameters;

wherein the program descriptions define the devices on a single bus by using a run method of the Java program language and define clock synchronizations of the devices by using barrier synchronizations;

wherein in the run method, program codes which are to be executed in a thread constituting a multi-thread are described,

wherein restrictions are imposed on the program descriptions which are an inhibition of dynamic instantiation restriction and an inhibition of a start method call from the run method restriction by employing a Java program language,

wherein the intermediate expression comprises a temporal automaton and a concurrent control flow flag generated by expressing the start of the "synchronized" operation as a node which is labeled as "Begin sync" and the end thereof as a node which is labeled as "End sync",

wherein the temporal automaton is converted from the concurrent control flow flag in which a part held between description the "Begin sync" and the "End sync" are identified, and is set as a "sync block", a clock boundary node which does not exist in the "sync" block is set as a state allotment candidate, the state allotment candidates obtained are allotted so as not to concur, and a section from each state to another state is traversed by a Depth First Search, a transition corresponding to the "sync" block is detected for the automaton and is set as a "sync" transition, and the number of states is decreased by collecting into one transition, transitions which are not successive transitions, and

wherein parametric model checking is performed using the temporal automaton for the parameter generation.

7. (Canceled)